

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED AKA on 9.6

APPLICATION NO.
09/663021

CONT/PRIOR
D

CLASS
257

SUBCLASS
750

ART UNIT
2814

EXAMINER

APPLICANTS

Kai Young

Self-aligned semiconductor interconnect barrier and manufacturing method therefor

PTO-2040
12/29

	CORRESPONDENCE						
	SERIAL NO.	REG. NO.	PATENT NO.				
I am the owner of this patent. Assigning to _____ (Name) In full payment of The fee term of this grant (Date) and extend beyond the expiration date of U.S. Patent No. _____ _____ _____	(Assistant Examiner)	(Date)	NOTICE OF ALLOWANCE GRANTED <hr/> <div align="center"> ISSUE FEE </div> <table border="1"> <thead> <tr> <th>Amount Due</th><th>Date Paid</th></tr> </thead> <tbody> <tr> <td> </td><td> </td></tr> </tbody> </table>	Amount Due	Date Paid		
	Amount Due	Date Paid					
(Primary Examiner)	(Date)	ISSUE BATCH NUMBER <hr/> <p>WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 189 and 602. Penalties outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.</p>					
(Legal Instruments Examiner)	(Date)						

Form PTO-424
(Rev. 8/73)

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM
(Attached in packet on right page(s))

(FACE)